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Jacqueline Chame, Michel Dubois

 June 1993 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1993 ACM SIGMETRICS conference on Measurement and modeling of computer systems**, Volume 21 Issue 1

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James R. Goodman

 August 1998 **25 years of the international symposia on Computer architecture (selected papers)**

Full text available: pdf(1.08 MB)

Additional Information: [full citation](#), [references](#), [index terms](#)3 [Modifying VM hardware to reduce address pin requirements](#)

Matthew Farrens, Arvin Park, Gary Tyson

 December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture**, Volume 23 Issue 1-2

Full text available: pdf(607.69 KB)

Additional Information: [full citation](#), [references](#), [index terms](#)4 [Organization and performance of a two-level virtual-real cache hierarchy](#)

W. H. Wang, J.-L. Baer, H. M. Levy

 April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the 16th annual international symposium on Computer architecture**, Volume 17 Issue 3

Full text available: pdf(1.01 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We propose and analyze a two-level cache organization that provides high memory bandwidth. The first-level cache is accessed directly by virtual addresses. It is small, fast, and, without the burden of address translation, can easily be optimized to match the processor speed. The virtually-addressed cache is backed up by a large physically-addressed cache; this second-level cache provides a high hit ratio and greatly reduces memory traffic. We show how the second-level cache can be easily e ...

5 [Eliminating the address translation bottleneck for physical address cache](#)

Tzi-cker Chiueh, Randy H. Katz

 September 1992 **ACM SIGPLAN Notices , Proceedings of the fifth international**


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